AMENDMENTS TO THE ABSTRACT

Please add the following paragraph for the abstract:

Noise-reducing transistor arrangement having first and second field effect transistors (FETs) having source terminals coupled together, drain terminals coupled together, and control terminals for application of a first or second signal. A clock generator unit is configured to provide the first and second signals alternately to the FETs with an alternating frequency which is at least as great as the cut-off frequency of the noise characteristic of the FETs, or with a reciprocal alternating frequency which is less than a mean lifetime of an occupation state of a defect in the boundary region between channel region and gate insulating layer of the FETs. The first signal is applied to the control terminal of the first FET and, simultaneously, the second signal to the control terminal of the second FET. The second signal is applied to the control terminal of the first FET and, simultaneously, the first signal to the control terminal of the second FET.